

Regionální inovační centrum elektrotechniky  
Fakulta elektrotechnická  
Západočeská univerzita v Plzni

## Základy generování cílového SW ze Simulinku

*Mikroprocesorové řízení pohonů 2*

Jakub Talla

- 1) Podpora cílových platforem
- 2) Simulink a HW periferie
- 3) Scheduling
- 4) Code replacement optimalizace (HW specifická)

# Podpora cílových platforem

## Podpora cílových platforem

- Umožňuje konfigurovat HW periferie
- Umožňuje nastavení HW interruptů (přerušení)
- Umožňuje specifickou optimalizaci kódu
- Umožňuje spolupráci s vývojovým prostředím mikrokontroléru (např. CCS)

## Podporované cílové platformy dle firem:

### 3D Robotics

- Advantech
- Altium
- Analog Devices
- Android
- Apple
- Arduino
- ARM
- Atmel
- Avnet
- B&R
- BeagleBoard
- Data Translation
- dSPACE
- Eclipse

- Ettus Research
- Freescale
- Green Hills Software
- Humusoft
- Infineon
- Intel
- Keithley Instruments
- LEGO
- Linux
- Measurement Computing
- Microchip
- Microsoft
- National Instruments
- NVIDIA

- NXP
- Parrot
- Quanser
- Raspberry Pi
- Renesas
- Robot Operating System
- RTI
- Speedgoat
- STMicroelectronics
- **Texas Instruments**
- TTi
- Vector
- Vex Robotics
- Xilinx

## Podporované cílové platformy firmy Texas Instrument:

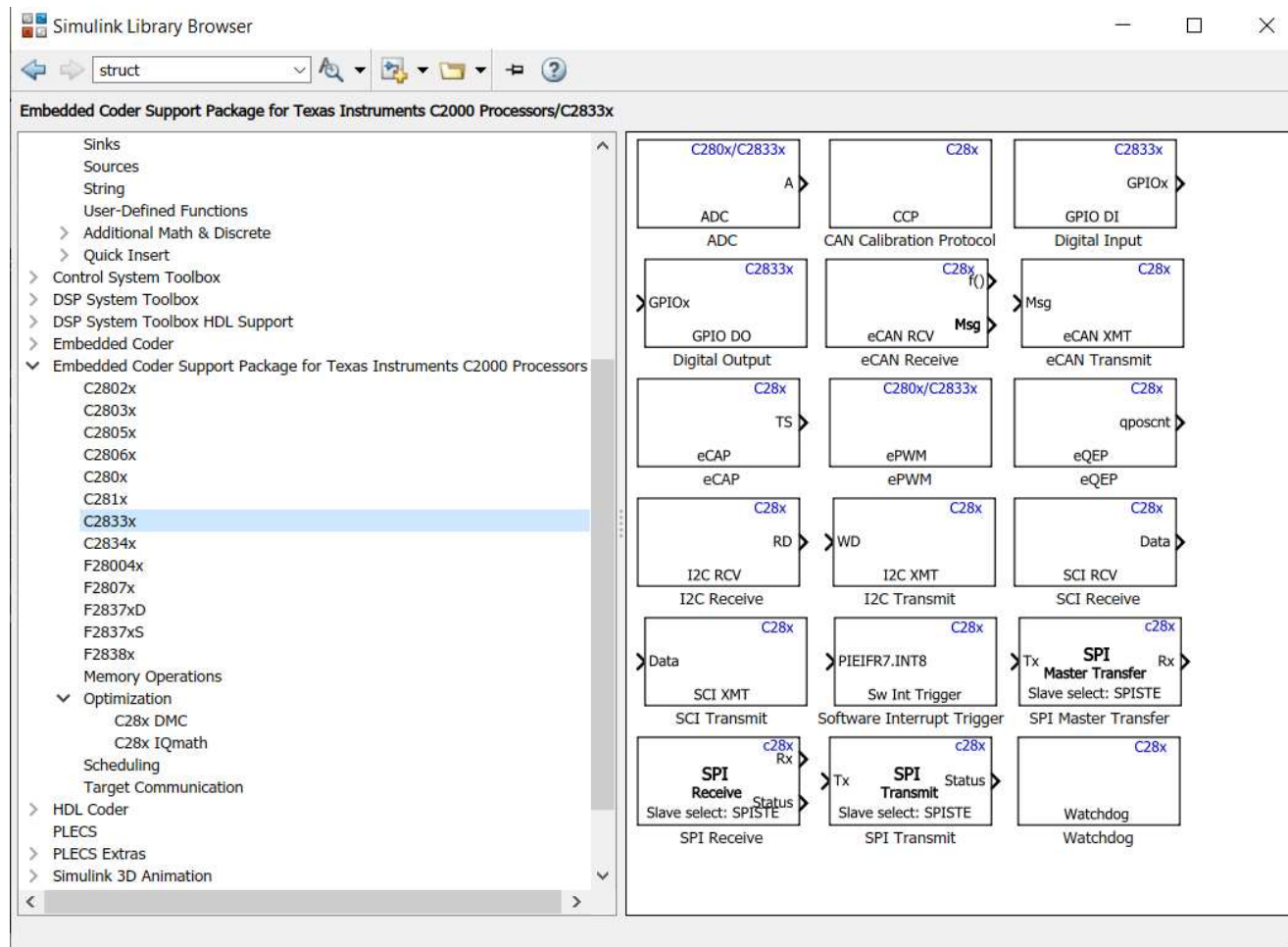
Microcontrollers	ARM Based Processors	Digital Signal Processors
MSP430™	Tiva™ C Series – M4 Stellaris® Cortex™-M3	C6000™ Power Optimized
<div style="border: 1px solid black; padding: 2px;">           C2000™            • Delfino™            • Piccolo™         </div>	TMS570 Cortex™-R4	C5000™ Ultra Low Power
	Sitara™	KeyStone Multicore
	Cortex™-A8 and ARM9®	KeyStone Multicore DSP+ARM
	KeyStone™	C6000™ Multicore
	OMAP Smart Multicore Processors with Cortex-A8, A9, and A15	

## Podporované cílové mikrokontroléry série TMS320C2000 firmy Texas Instrument:

Processor Family	Processors
TI Delfino F28377S LaunchPad	F28377S
TI Delfino F2837xS	F28379S, F28377S, F28376S, F28375S, and F28374S
TI Delfino F28379D LaunchPad	F28379D
TI Delfino F2837xD	F28379D, F28377D, F28376D, F28375D, and F28374D
TI Delfino F2833x	F28335, F28334, and F28332
TI Delfino C2834x	C28346, C28345, C28344, C28343, C28342, and C28341
TI Piccolo F280049C LaunchPad	F280049C
TI Piccolo F28004x	F280049M, F280049C, F280049, F280048C, F280048, F280045, F280041C, F280041, F280040C, and F280040
TI Piccolo F2807x	F28075 and F28074
TI Piccolo F2806x	F28069M, F28069, F28068, F28067, F28066, F28065, F28064, F28063, and F28062
TI Piccolo F28069M LaunchPad	F28069M
TI Piccolo F2805x	F28055, F28054, F28053, F28052, F28051, and F28050
TI Piccolo F2803x	F28035, F28034, F28033, F28032, F28031, and F28030
TI Piccolo F2802x	F28027, F28026, F28023, F28022, F28021, F28020, and F280200
TI Piccolo F28027/F28027F LaunchPad	F28027
TI F280x	F2809, F2808, F2806, F2802, F2801, F28016, and F28015
TI F28044	F28044
TI F281x	F2812, F2811, and F2810
TI F2838x	F28388D, F28388S, F28386D, F28386S, F28384D, and F28384S

# Simulink a HW periferie

## Bloky HW periferií



Simulink Library Browser  
 struct

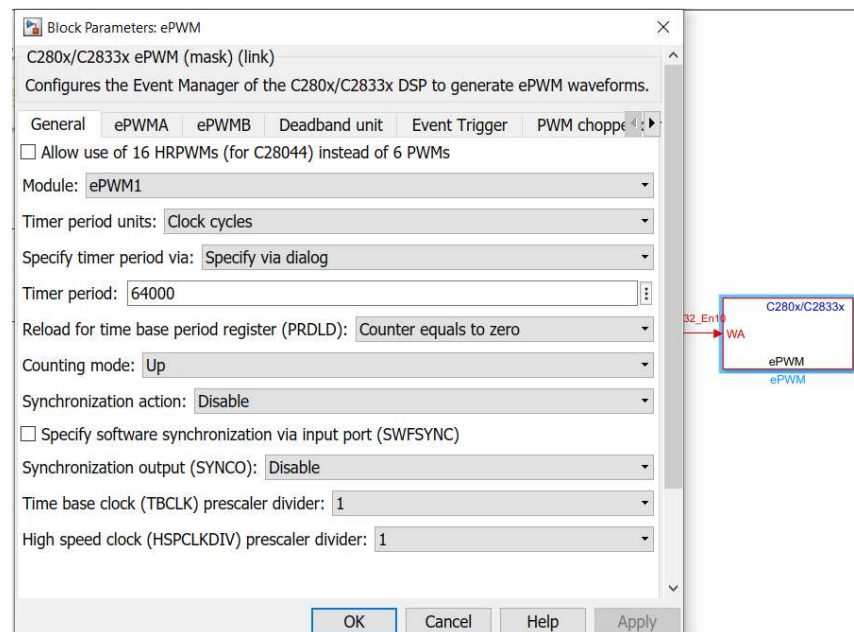
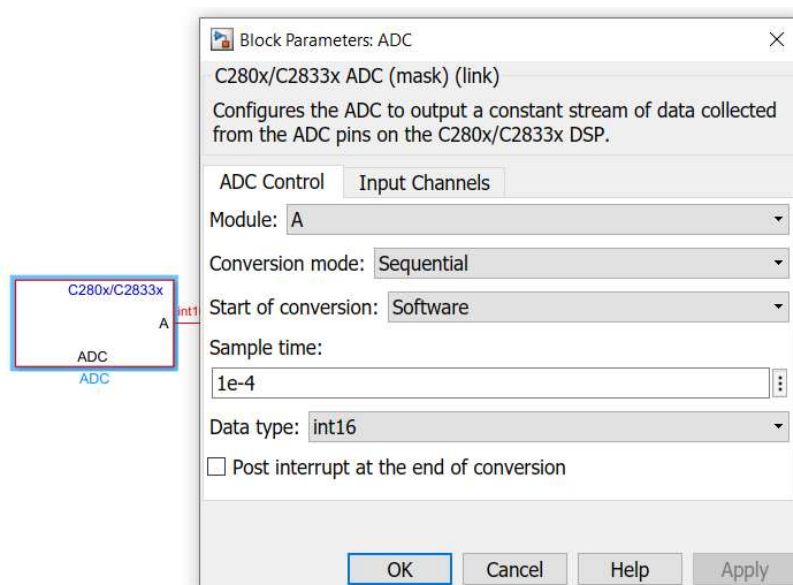
**Embedded Coder Support Package for Texas Instruments C2000 Processors/C2833x**

- Sinks
- Sources
- String
- User-Defined Functions
- > Additional Math & Discrete
- > Quick Insert
- > Control System Toolbox
- > DSP System Toolbox
- > DSP System Toolbox HDL Support
- > Embedded Coder
- ✓ Embedded Coder Support Package for Texas Instruments C2000 Processors
  - C2802x
  - C2803x
  - C2805x
  - C2806x
  - C280x
  - C281x
  - C2833x**
  - C2834x
  - F28004x
  - F2807x
  - F2837xD
  - F2837xS
  - F2838x
  - Memory Operations
  - ✓ Optimization
    - C28x DMC
    - C28x IQmath
  - Scheduling
  - Target Communication
- > HDL Coder
- PLECS
- > PLECS Extras
- > Simulink 3D Animation

Hardware peripheral blocks displayed:

- ADC (C280x/C2833x)
- CCP (C28x)
- GPIOx (C2833x)
- GPIO DI (C2833x)
- GPIO DO (C2833x)
- Digital Output (C2833x)
- eCAN RCV (C28x)
- eCAN Receive (C28x)
- eCAN XMT (C28x)
- eCAN Transmit (C28x)
- eCAP (C28x)
- eCAP (C280x/C2833x)
- ePWM (C28x)
- ePWM (C280x/C2833x)
- eQEP (C28x)
- eQEP (C280x/C2833x)
- qposcnt (C28x)
- I2C RCV (C28x)
- I2C Receive (C28x)
- I2C XMT (C28x)
- I2C Transmit (C28x)
- SCI RCV (C28x)
- SCI Receive (C28x)
- SCI XMT (C28x)
- SCI Transmit (C28x)
- Software Interrupt Trigger (C28x)
- SPI Master Transfer (C28x)
- SPI Master Transfer (C28x)
- SPI Receive (C28x)
- SPI Receive (C28x)
- SPI Transmit (C28x)
- SPI Transmit (C28x)
- Watchdog (C28x)
- Watchdog (C28x)

## Bloky HW periferií - konfigurace



### Tvorba vlastního driveru:

[https://www.mathworks.com/help/supportpkg/raspberrypi/device-driver-blocks.html?s\\_tid=CRUX\\_lftnav](https://www.mathworks.com/help/supportpkg/raspberrypi/device-driver-blocks.html?s_tid=CRUX_lftnav)

## Konfigurace HW periferií

[Summary](#)

[Subsystem Report](#)

[Code Interface Report](#)

[Traceability Report](#)

[Static Code Metrics Report](#)

[Code Replacements Report](#)

[Coder Assumptions](#)

### Generated Code

[ - ] Main file

[ert\\_main.c](#)

[ - ] Model files

[prednaska10b.c](#)

[prednaska10b.h](#)

[ + ] Utility files (1)

```

250 /* Model initialize function */
251 void prednaska10b_initialize(void)
252 {
253     /* Registration code */
254
255     /* initialize real-time model */
256     (void) memset((void *)rtM, 0,
257                 sizeof(RT_MODEL));
258
259     /* states (dwork) */
260     (void) memset((void *)&rtDW, 0,
261                 sizeof(DW));
262
263     /* Start for S-Function (c280xpwm): '<Root>/ePWM' */
264
265     /*** Initialize ePWM1 modules ***/
266     {
267         /*-- Setup Time-Base (TB) Submodule --*/
268         EPwm1Regs.TBPRD = 64000;
269
270         /* // Time-Base Control Register
271            EPwm1Regs.TBCTL.bit.CTRMODE = 0;           // Counter Mode
272            EPwm1Regs.TBCTL.bit.SYNCSEL = 3;           // Sync output select
273            EPwm1Regs.TBCTL.bit.PRDL = 0;             // Shadow select
274
275            EPwm1Regs.TZCTL.all = (EPwm1Regs.TZCTL.all & ~0xF) | 0xF;
276
277            /* // Trip-Zone Enable Interrupt Register
278            EPwm1Regs.TZEINT.bit.OST = 0;             // Trip Zones On
279            EPwm1Regs.TZEINT.bit.CBC = 0;             // Trip Zones Cn.
280            */
281            EPwm1Regs.TZEINT.all = (EPwm1Regs.TZEINT.all & ~0x6) | 0x0;
282            EDIS;
283        }
284
285     /* Start for S-Function (c280xadc): '<Root>/ADC' */
286     if (adcInitFlag == 0) {
287         InitAdc();
288         adcInitFlag = 1;
289     }
290
291     config_ADC_A (0U, 0U, 0U, 0U, 0U);
292 }
293

```

## V periodicky volané funkci

```

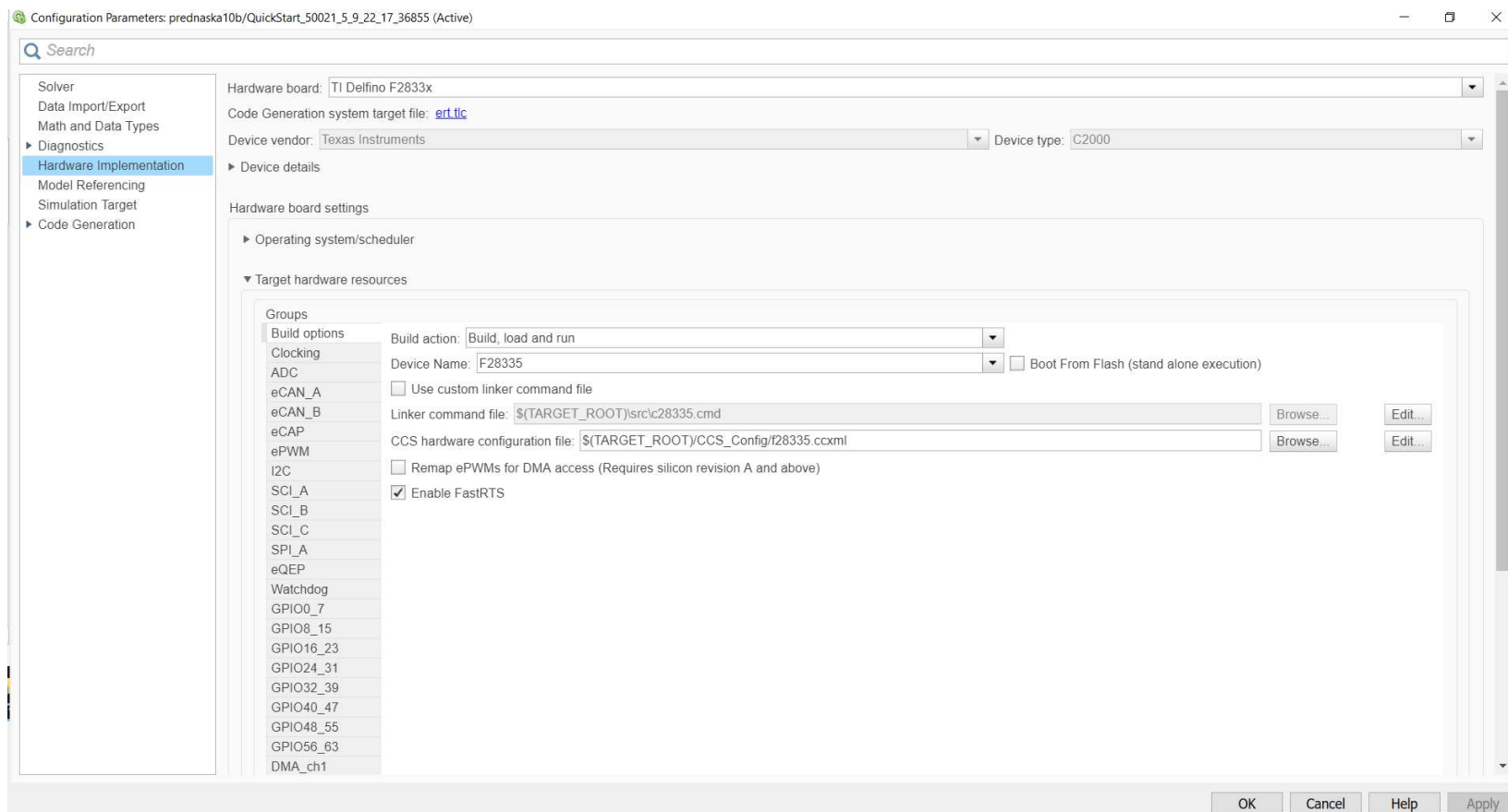
/*-- Update CMPA value for ePWM1 --*/
{
    _iq10 InPortValue = rtDW.IQNXIQN;
    EPwm1Regs.CMPA.half.CMPA = (uint16_T)((_IQ10mpyI32int(InPortValue,
    EPwm1Regs.TBPRD) * 0.01));
}

/* S-Function (c280xadc): '<Root>/ADC' */
{
    AdcRegs.ADCR2.bit.RST_SEQ1 = 1; /* Reset SEQ1 module*/
    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1; /*Clear INT sequencer*/
    AdcRegs.ADCR2.bit.SOC_SEQ1 = 1; /* Software Trigger*/
    while (AdcRegs.ADCST.bit.INT_SEQ1 == 0) {
        } /*Wait for Sequencer INT bit to clear */

    asm(" RPT #11 || NOP");
    rtDW.ADC = (AdcRegs.ADCRESULT0) >> 4;
}

```

## Další konfigurace projektu a HW periferií



Configuration Parameters: prednaska10b/QuickStart\_50021\_5\_9\_22\_17\_36855 (Active)

Search

Solver  
Data Import/Export  
Math and Data Types  
Diagnostics  
**Hardware Implementation**  
Model Referencing  
Simulation Target  
Code Generation

Hardware board: TI Delfino F2833x  
Code Generation system target file: [ert.tlc](#)  
Device vendor: Texas Instruments Device type: C2000

Device details

Hardware board settings

Operating system/scheduler

Target hardware resources

Groups

Build options Build action: Build, load and run

Clocking Device Name: F28335  Boot From Flash (stand alone execution)

ADC  Use custom linker command file

eCAN\_A Linker command file: \$(TARGET\_ROOT)/src/c28335.cmd Browse... Edit...

eCAN\_B

eCAP CCS hardware configuration file: \$(TARGET\_ROOT)/CCS\_Config/f28335.ccxml Browse... Edit...

ePWM  Remap ePWMs for DMA access (Requires silicon revision A and above)

I2C  Enable FastRTS

SCI\_A  
SCI\_B  
SCI\_C  
SPI\_A  
eQEP  
Watchdog  
GPIO0\_7  
GPIO8\_15  
GPIO16\_23  
GPIO24\_31  
GPIO32\_39  
GPIO40\_47  
GPIO48\_55  
GPIO56\_63  
DMA\_ch1

OK Cancel Help Apply

# Scheduling

## (harmonogram časování)

Simulink umožňuje tři typy událostí:

## BASE RATE Synchronní událost

- V Simulinku jako časové smyčky, HW řešen většinou jako interrupt časovače

Základní krok simulace nastaví interrupt časovače a v něm SW řeší jednotlivé časové smyčky podle priorit od nejmenšího kroku do největšího

## HW INTERRUPT Obecně asynchronní událost

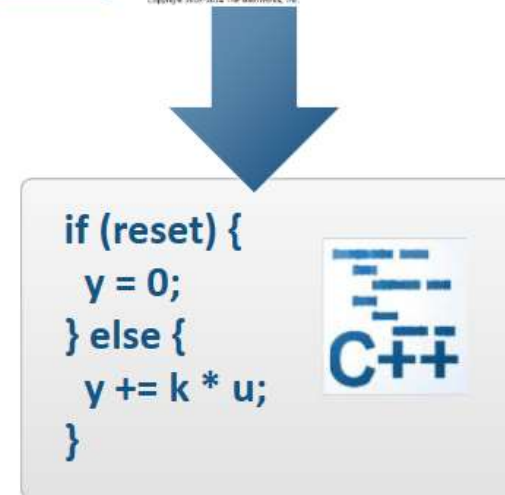
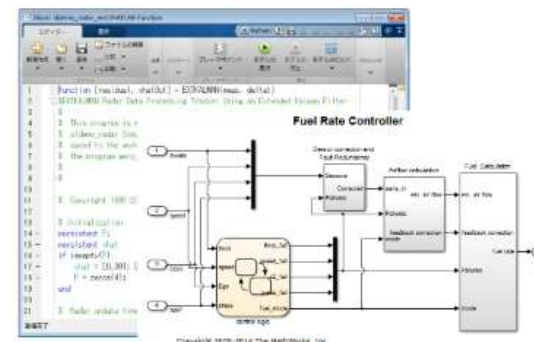
- V Simulinku řešen jako volání funkce

V rámci bloku HW interruptu lze nastavit priority, přerušitelnost apod. Řešen jako asynchronní funkce

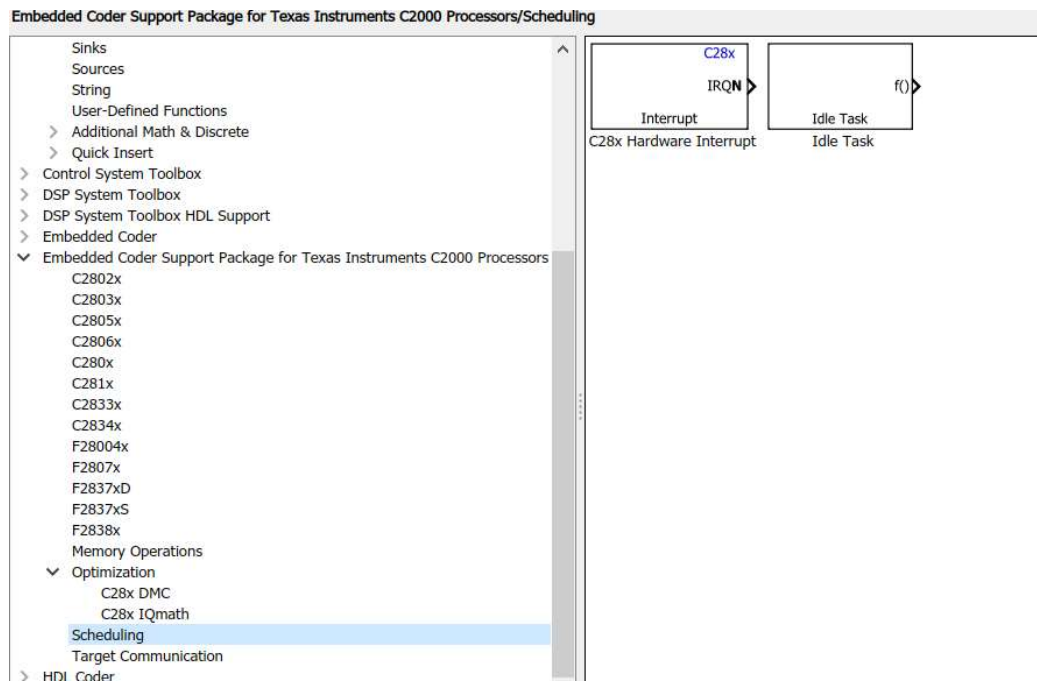
## IDLE TASK Asynchronní s nízkou prioritou

- V Simulinku řešen jako volání funkce

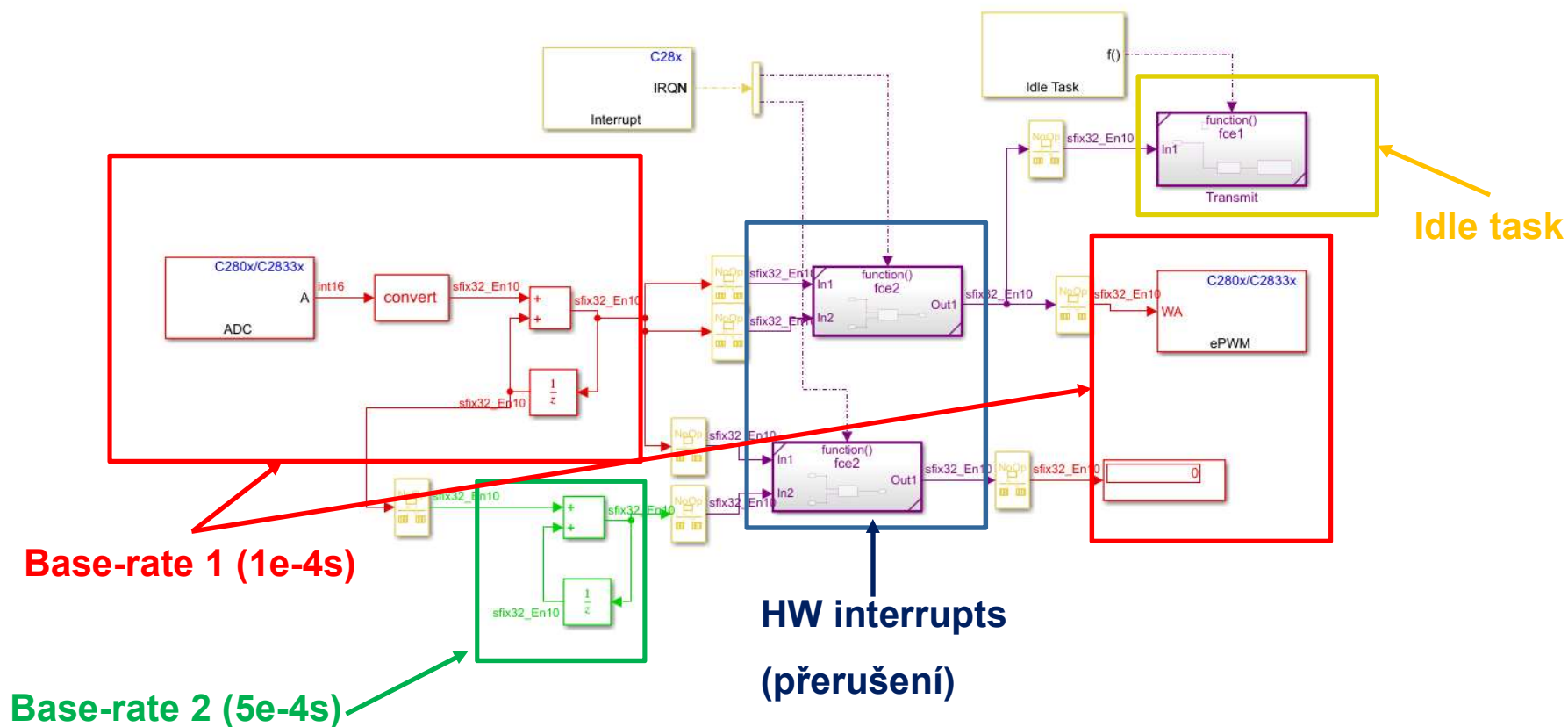
Úloha volaná mimo HW interrupt v nekonečné while smyčce. Priority určují pořadí volání funkcí.



## Scheduling = řízení událostí (HW přerušení apod.)



## Simulink umožňuje mix všech typů časování



## Soubor Main

```
24 volatile int IsrOverrun = 0;
25 static boolean_T OverrunFlag = 0;
26 void rt_OneStep(void) ←
27 {
28
41 }
45 int main(void) ←
46 {
47     float modelBaseRate = 0.0001;
48     float systemClock = 150;
49
50     /* Initialize variables */
51     stopRequested = false;
52     runModel = false;
53     c2000_flash_init();
54     init_board();
55
56     prednaska10b_initialize();
57     configureTimer0(modelBaseRate, systemClock);
58     runModel =
59         rtmGetErrorStatus(rtm) == (NULL);
60     enableTimer0Interrupt();
61     enable_interrupts();
62     globalInterruptEnable();
63
64     while (runModel) { ←
65         stopRequested = !(
66             rtmGetErrorStatus(rtm) == (NULL));
67     }
68
69     /* Disable rt_OneStep() here */
70     globalInterruptDisable();
71     return 0;
72 }
73
74
75
76
77
78
79 }
80
```

**rt\_OneStep - Funkce Base-rate  
základní časové smyčky (volaná  
přerušením Timeru či ADC)**

**main**

**Inicializace HW a modelu (software)**

**Nekonečná while smyčka v ní  
může být volání idle funkce**

## rt\_OneStep funkce řídící multitasking základních base-rate časových smyček

```

29 void rt_OneStep(void)
30 {
31     boolean_T eventFlags[2];
32
33     /* Check base rate for overrun */
34     if (isRateRunning[0]++) {
35         IsrOverrun = 1;
36         isRateRunning[0]--;          /* c
37         return;
38     }
39
40     enableTimer0Interrupt();
41     prednaska10b_step0();
42
43     /* Get model outputs here */
44     disableTimer0Interrupt();
45     * enableTimer0Interrupt();
46
47
48     /* Step the model for subrate "1" */
49     switch (1)
50     {
51     case 1 :
52         prednaska10b_step1();
53
54         /* Get model outputs here */
55         break;
56
57     default :
58         break;
59     }
60
61     disableTimer0Interrupt();
62
63     static void rate_monotonic_scheduler(void)
64     {
65         /* Compute which subrates run during the next base time step. Subrates
66          * are an integer multiple of the base rate counter. Therefore, the subtask
67          * counter is reset when it reaches its Limit (zero means run).
68          */
69         (rtM->Timing.TaskCounters.TID[1])++;
70         if ((rtM->Timing.TaskCounters.TID[1]) > 4) { /* Sample time: [0.0005s, 0.0s] */
71             rtM->Timing.TaskCounters.TID[1] = 0;
72         }
73     }
74
75     /* Model step function for TID0 */
76     void prednaska10b_step0(void)          /* Sample time: [0.0001s, 0.0s] */
77     {
78         {                                  /* Sample time: [0.0001s, 0.0s] */
79             rate_monotonic_scheduler();
80         }
81
82         /* UnitDelay: '<Root>/Unit Delay' */
83         rtDW.UnitDelay = rtDW.UnitDelay_DSTATE;
84
85         /* S-Function (c280xpwm): '<Root>/ePWM' */
86
87         /*-- Update CMPA value for ePWM1 --*/
88         {
89             _iq10 InPortValue = rtDW.IQNxIQN;
90             EPwm1Regs.CMPA.half.CMPA = (uint16_T)((_IQ10mpyI32int(InPortValue,
91                 EPwm1Regs.TBPRD) * 0.01));
92         }
93     }
94

```

## Base-rate HW přerušení od Timeru konfigurace v souboru c2833xSchedulerTimer0.c

Model files

- [prednaska10b.c](#)
- [prednaska10b.h](#)

Utility files (1)

Interface files (1)

Other files

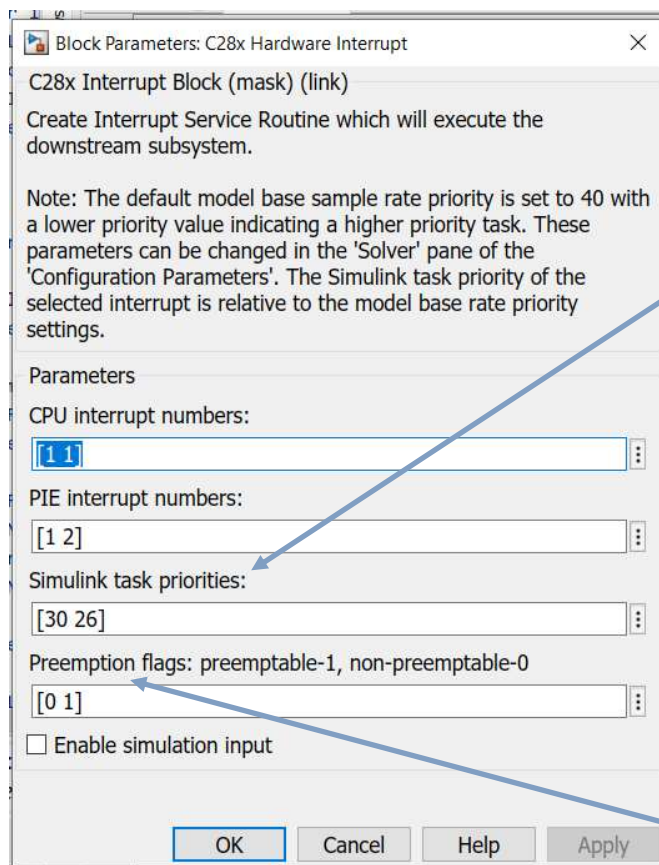
- [DSP2833x\\_ADC\\_cal.asm](#)
- [DSP2833x\\_CodeStartBranch.asm](#)
- [DSP2833x\\_CpuTimers.c](#)
- [DSP2833x\\_DMA.c](#)
- [DSP2833x\\_DefaultIsr.c](#)
- [DSP2833x\\_GlobalVariables.c](#)
- [DSP2833x\\_MemCopy.c](#)
- [DSP2833x\\_PieCtrl.c](#)
- [DSP2833x\\_PieVect.c](#)
- [DSP2833x\\_SysCtrl.c](#)
- [DSP2833x\\_usDelay.asm](#)
- [MW\\_c28xx\\_board.c](#)
- [MW\\_c28xx\\_csl.c](#)
- [MW\\_c28xx\\_pie.h](#)

File: [c2833xSchedulerTimer0.c](#)

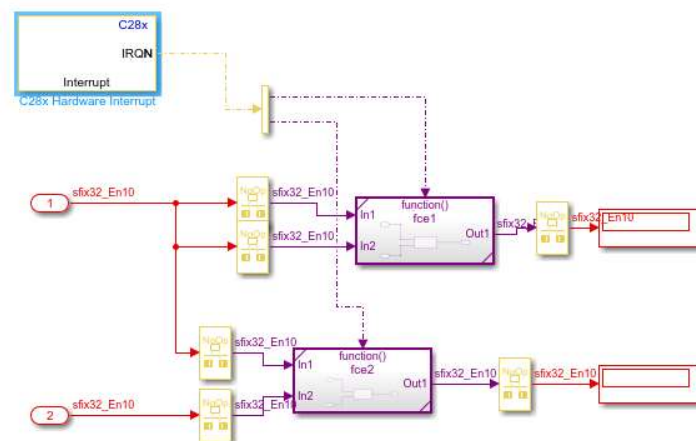
```

1  #include <stdbool.h>
2
3  #include "DSP2833x_Device.h"
4  #include "DSP2833x_CpuTimers.h"
5  #include "MW_c28xx_pie.h"
6
7  extern void rt_OneStep(void);
8
9  interrupt void TINT0_isr(void)
10 {
11     #ifndef PIEMASK0
12         volatile unsigned int PIEIER1_stack_save = PieCtrlRegs.PIEIER1.all;
13     #endif
14
15     asm(" RPT #5 || NOP");           /* wait 5 cycles */
16     IFR &= ~IFRMASK;                 /* eventually disable lower/equal */
17     PieCtrlRegs.PIEACK.all = IFRMASK; /* ACK to allow other interrupts fi
18
19     IER |= 1;
20     EINT;                             /* global interrupt enable */
21     rt_OneStep();
22     DINT;                             /* disable global interrupts during conti
23
24     ...
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## Hardware Interrupt (HW přerušení)



**Base rate task priorita 40, čím nižší číslo tím vyšší priorita**



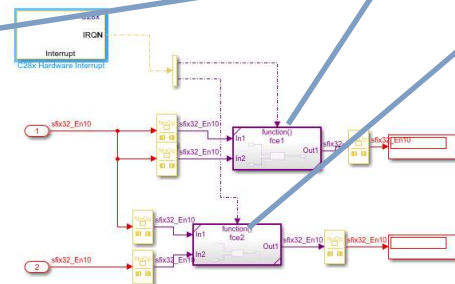
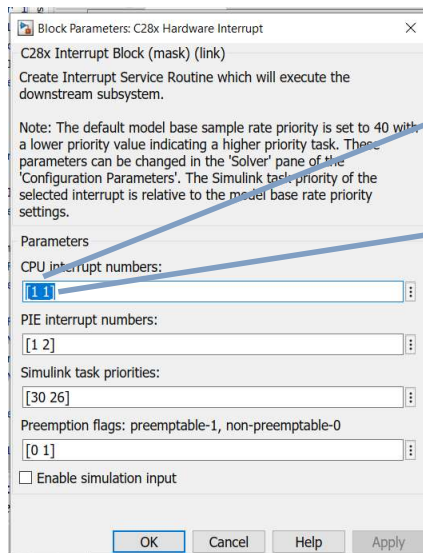
**Přerušitelnost přerušením s vyšší prioritou (0 ne 1 ano)**

## Tabulka přerušení (součást help)

PIE and CPU Interrupt Numbers for F280x, F2802x, F2803x, F2805x, F2806x, F2833x, F28M35x, and F28M36x Processors

PIE → CPU ↓	1	2	3	4	5	6	7	8
1	SEQ1INT (ADC) / ADCINT1	SEQ2INT (ADC) / ADCINT2	Reserved	XINT1	XINT2	ADCINT / ADCINT9	TINT0 (TIMER 0)	WAKEINT (LPM/WD)
2	EPWM1_TZINT	EPWM2_TZINT	EPWM3_TZINT	EPWM4_TZINT	EPWM5_TZINT	EPWM6_TZINT	EPWM7_TZINT	EPWM8_TZINT
3	EPWM1_INT	EPWM2_INT	EPWM3_INT	EPWM4_INT	EPWM5_INT	EPWM6_INT	EPWM7_INT	EPWM8_INT
4	ECAP1_INT	ECAP2_INT	ECAP3_INT	ECAP4_INT	ECAP5_INT	ECAP6_INT	EPWM10_TZINT / HRCAP1_INT	EPWM9_TZINT / HRCAP2_INT
5	EQEP1_INT	EQEP2_INT	EQEP3_INT	HRCAP3_INT	HRCAP4_INT	Reserved	EPWM10_INT	EPWM9_INT
6	SPIRXINTA (SPI-A)	SPITXINTA (SPI-A)	SPIRXINTB (SPIB_RX) / MRINTB (McBSP-B)	SPITXINTB (SPIB_TX) / MXINTB (McBSP-B)	SPIRXINTC (SPI-C) / MRINTA (McBSP-A_RX)	SPITXINTC (SPI-C) / MXINTA (McBSP-A_TX)	SPIRXINTD (SPI-D) / EPWM12_TZINT	SPITXINTD (SPI-D) / EPWM11_TZINT
7	DINTCH1 (DMA1)	DINTCH2 (DMA2)	DINTCH3 (DMA3)	DINTCH4 (DMA4)	DINTCH5 (DMA5)	DINTCH6 (DMA6)	EPWM12_INT	EPWM11_INT
8	I2CINT1A	I2CINT2A	Reserved	Reserved	SCIRXINTC (SCI-C)	SCITXINTC (SCI-C)	Reserved	Reserved
9	SCIRXINTA (SCIA_RX)	SCITXINTA (SCIA_TX)	SCIRXINTB (SCIB_RX) / LINA_INT0	SCITXINTB (SCIB_TX) / LINA_INT1	ECAN0INTA (CANA_1)	ECAN1INTA (CANA_2)	ECAN0INTB (CANB_1)	ECAN1INTB (CANB_2)
10	EPWM9_TZINT / ADCINT1	EPWM10_TZINT / ADCINT2	EPWM11_TZINT / ADCINT3	EPWM12_TZINT / ADCINT4	EPWM13_TZINT / ADCINT5	EPWM14_TZINT / ADCINT6	EPWM15_TZINT / ADCINT7	EPWM16_TZINT / ADCINT8
11	CLA1_INT1 / EPWM9_INT7 / MTOCIPCINT1	CLA1_INT2 / EPWM10_INT / MTOCIPCINT2	CLA1_INT3 / EPWM11_INT / MTOCIPCINT3	CLA1_INT4 / EPWM12_INT / MTOCIPCINT4	CLA1_INT5 / EPWM13_INT	CLA1_INT6 / EPWM14_INT	CLA1_INT7 / EPWM15_INT	CLA1_INT8 / EPWM16_INT
12	XINT3	XINT4 / C28FLSINGERR	XINT5	XINT6 / C28RAMSINGERR	XINT7 / C28RAMACCVIOL	Reserved	LVF	LUF

## Hardware Interrupt (HW přerušení)

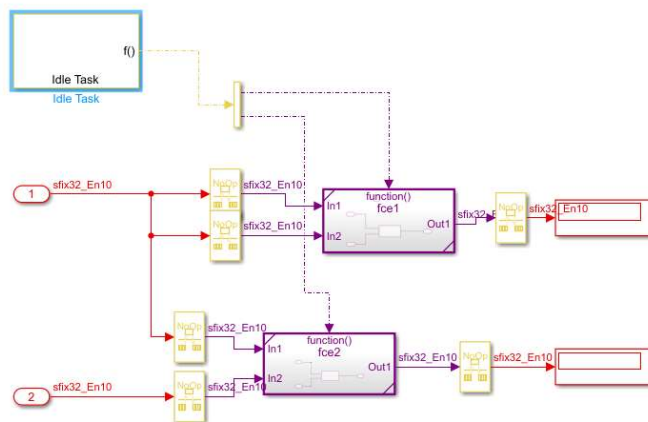
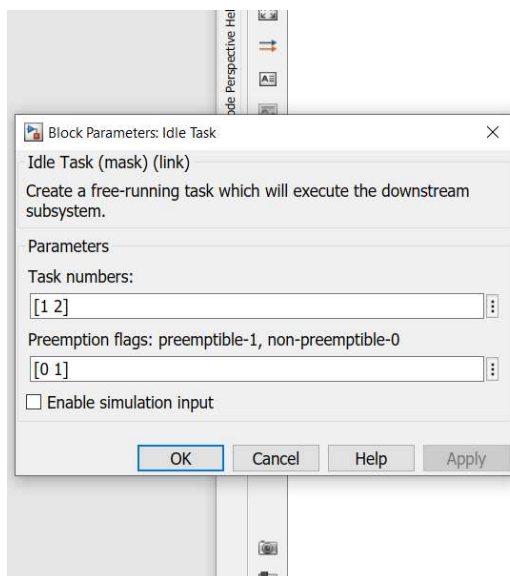


```

17 interrupt void SEQ1INT_isr(void)
18 {
19     isr_int1pie1_task_fcn();
20     EALLOW;
21     AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;
22     EDIS;
23     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
24                                     /* Acknowledge to receive more interrupts*/
25 }
26
27 interrupt void SEQ2INT_isr(void)
28 {
29     volatile unsigned int PIEIER1_stack_save = PieCtrlRegs.PIEIER1.all;
30     PieCtrlRegs.PIEIER1.all &= ~67;
31                                     /*disable group1 lower/equal priority interrupts*/
32     asm(" RPT #5 || NOP");           /*wait 5 cycles */
33     IFR &= ~1;                       /*eventually disable lower/equal priority pending interrupts*/
34     PieCtrlRegs.PIEACK.all = 1;
35                                     /*ACK to allow other interrupts from the same group to fire*/
36     IER |= 1;
37     EINT;                             /*global interrupt enable*/
38     isr_int1pie2_task_fcn();
39     DINT;
40     /* disable global interrupts during context switch, CPU will enable global interrupts of
41     PieCtrlRegs.PIEIER1.all = PIEIER1_stack_save;
42                                     /*restore PIEIER register that was modified*/
43     EALLOW;
44     AdcRegs.ADCST.bit.INT_SEQ2_CLR = 1;
45     EDIS;
46     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
47                                     /* Acknowledge to receive more interrupts*/
48 }
49

```

## IDLE task



[ - ] Main file

ert\_main.c

[ - ] Model files

prednaska10b.c

prednaska10b.h

```

55 enableTimer0Interrupt();
56 globalInterruptEnable();
57 while (runModel) {
58     stopRequested = !(
59         rtmGetErrorStatus(rtm) == (NULL));
60     idletask_num1();
61     idletask_num2();
62 }
  
```

```

17 void idletask_num1(void)
18 {
19     DINT; /* disable global interrupts*/
20     idle_num1_task_fcn();
21     EINT; /* reenale global interrupts*/
22 }
23
24 void idletask_num2(void)
25 {
26     idle_num2_task_fcn();
27 }
  
```

# Optimalizace - Code replacement

## Code replacement umožňuje náhradu obecných funkcí specifickými (např. HW optimalizovanými)

Configuration Parameters: prednaska10/QuickStart\_50021\_5\_8\_20\_49\_36518 (Active)

Search

- Solver
- Data Import/Export
- Math and Data Types
- ▶ Diagnostics
- Hardware Implementation
- Model Referencing
- Simulation Target
- ▼ Code Generation
  - Optimization
  - Report
  - Comments
  - Identifiers
  - Custom Code
  - Interface**
  - Code Style
  - Verification
  - Templates
  - Code Placement
  - Data Type Replacement

Software environment

Code replacement library: **None** Specify the code replacement library available to you

Shared code placement:

Support:  floating-point numbers  non-finite  absolute time  continuous

Code interface

Code interface packaging: Nonreusable function

Remove error status field in real-time model data structure

Data exchange interface

Array layout: Column-major

External functions compatibility for row-major code generation: error

Generate C API for:

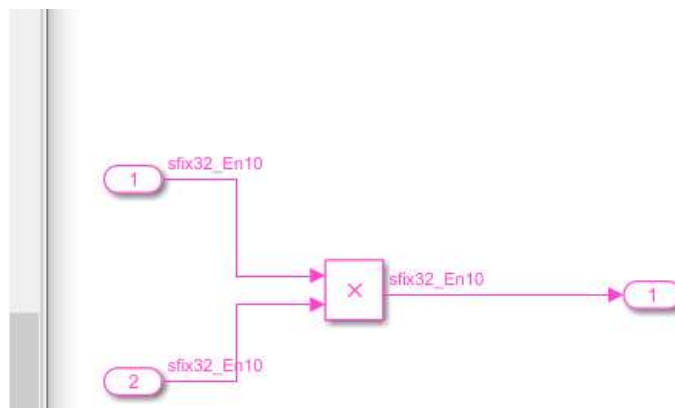
signals  parameters  states  root-level I/O

ASAP2 interface

## Code replacement lib. TI C28x

```

78 /* Model step function */
79 void Subsystem_step(void)
80 {
81   /* Outport: '<Root>/Out1' incorporates:
82    * Inport: '<Root>/In1'
83    * Inport: '<Root>/In2'
84    * Product: '<S1>/Product'
85   */
86   rtY.Out1 = __IQmpy(rtU.In1, rtU.In2, 10);
87 }
88
  
```

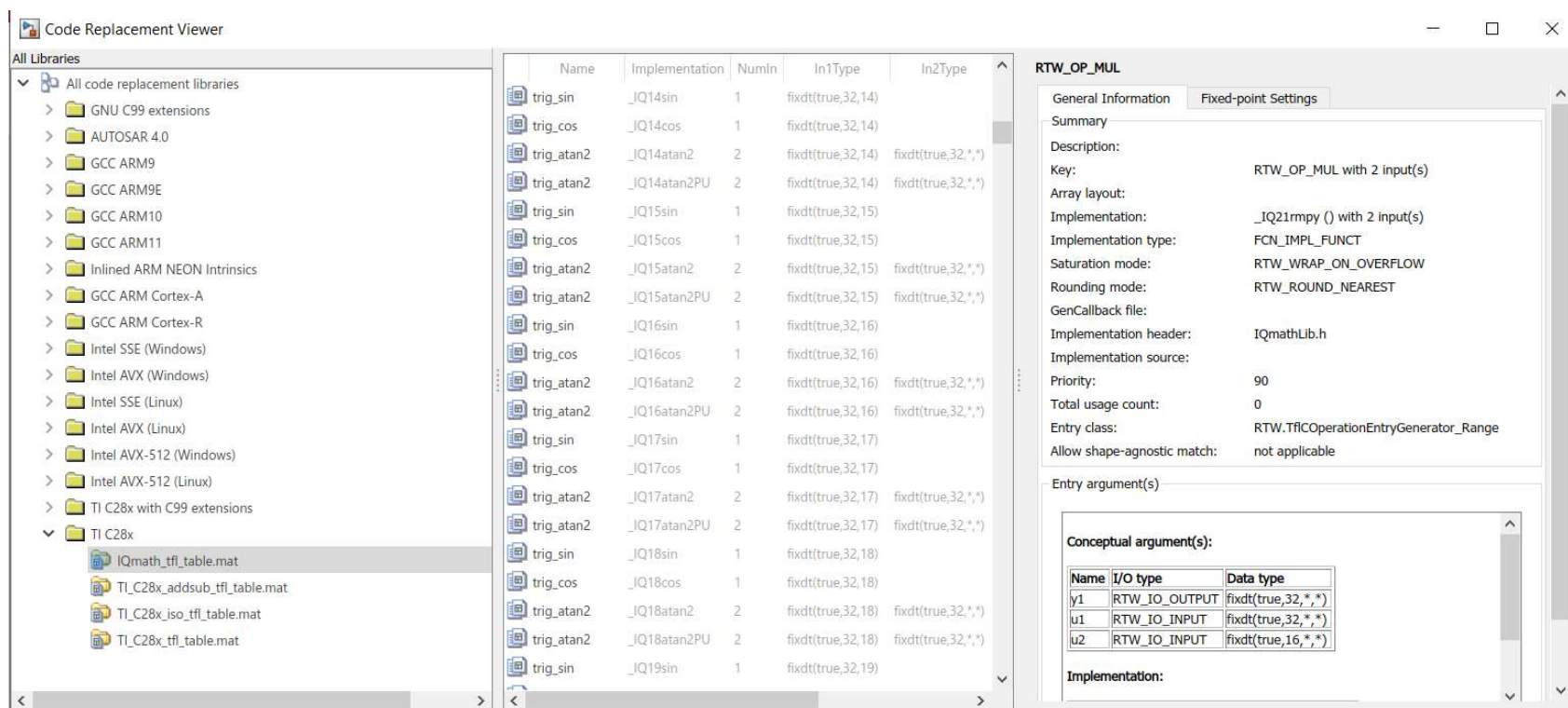


```

/* Model step function */
void Subsystem_step(void)
{
  /* Outport: '<Root>/Out1' incorporates:
  * Inport: '<Root>/In1'
  * Inport: '<Root>/In2'
  * Product: '<S1>/Product'
  */
  rtY.Out1 = (int32_T)((((int64_T)rtU.In1 * rtU.In2) >> 10U);
}
  
```

Code replacement lib. None

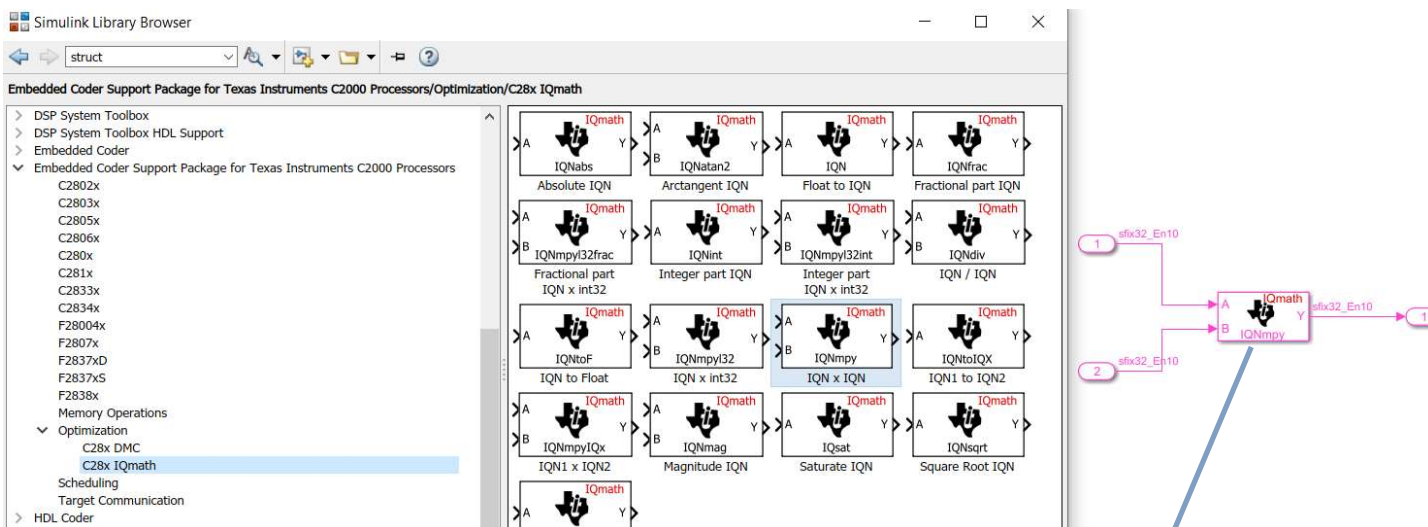
## Code replacement viewer (příkaz crviewer, vlastní knihovna příkazem crtool)



The screenshot displays the Code Replacement Viewer interface. On the left, a tree view shows 'All Libraries' with 'TI C28x' expanded to show 'IQmath\_tfl\_table.mat'. The center pane lists various trigonometric functions like 'trig\_sin', 'trig\_cos', and 'trig\_atan2' with their respective implementations and data types. The right pane shows the 'RTW\_OP\_MUL' function details, including its key, description, implementation type, and a table of conceptual arguments.

Name	I/O type	Data type
y1	RTW_IO_OUTPUT	fixdt(true,32,*,*)
u1	RTW_IO_INPUT	fixdt(true,32,*,*)
u2	RTW_IO_INPUT	fixdt(true,16,*,*)

## Použití specifických (optimalizovaných) bloků

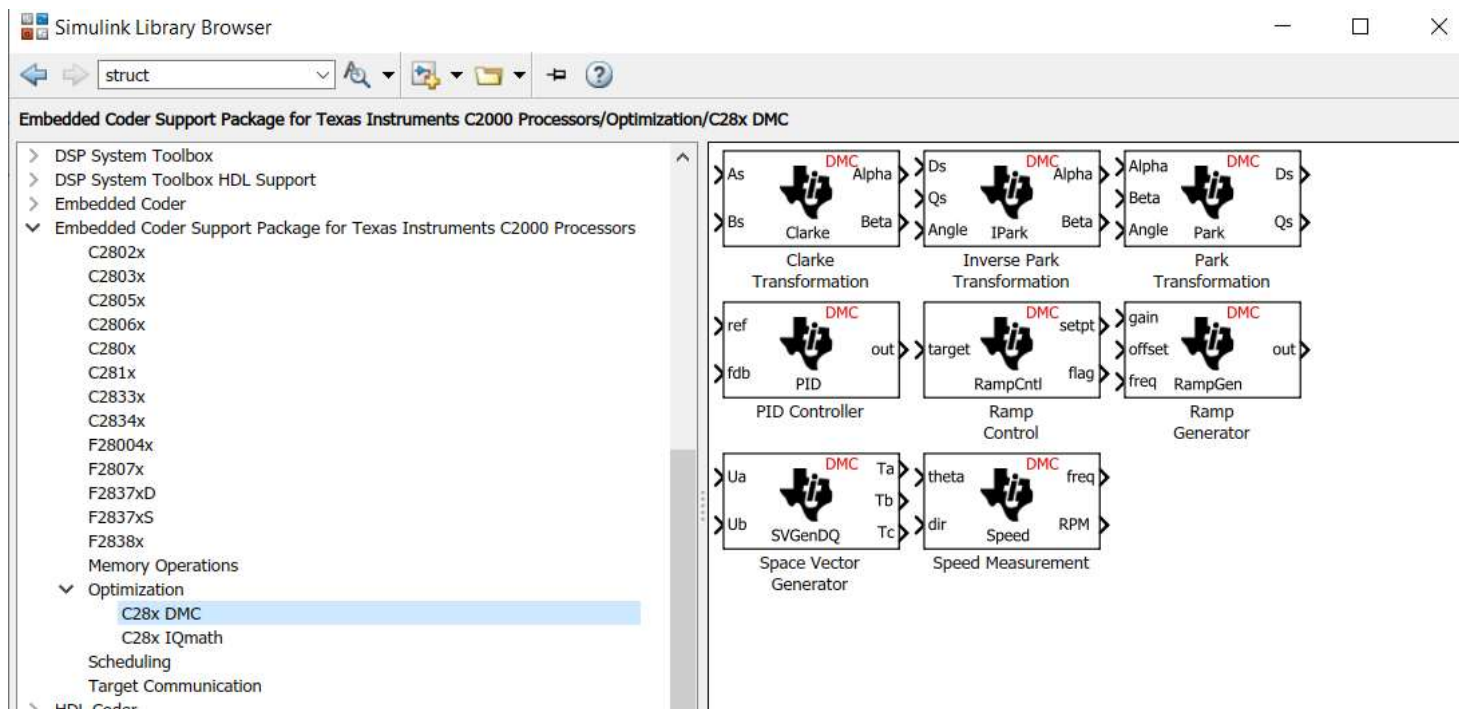


```

void Subsystem1_step(void)
{
  /* S-Function (stiiqmath_iqmpy): '<S1>/IQN x IQN' incorporates:
   * Inport: '<Root>/In1'
   * Inport: '<Root>/In2'
   * Outport: '<Root>/Out1'
   */

  /* C28x IQmath Library (stiiqmath_iqmpy) - '<S1>/IQN x IQN' */
  {
    rtY.Out1 = _IQ10mpy (rtU.In1, rtU.In2);
  }
}
  
```

## Použití specifických (optimalizovaných) bloků DMC knihovna



Regionální inovační centrum elektrotechniky  
Fakulta elektrotechnická  
Západočeská univerzita v Plzni

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